CLAIMS

What is claimed is:

1. A method comprising:

obtaining data to be written to a memory unit;

determining if the data is aligned, and

if the data is aligned, writing a first portion of a first block of the data to a first memory bank of the memory unit, and writing a second portion of the first block of the data to a second memory bank of the memory unit; and

if the data is not aligned, writing the first portion of the first block to the second memory bank and the second portion of the first block to the first memory bank.

2. The method of claim 1, in which:

if the data is aligned, writing the first portion of the first block to the first memory bank at a first address, and writing the second portion of the first block to the second memory bank at the first address; and

if the data is not aligned, writing the first portion of the first block to the second memory bank at a second address, and writing the second portion of the first block to the first memory bank at a third address.

3. The method of claim 1, in which the first portion and the second portion are written to the memory unit substantially simultaneously.

4. The method of claim 3, in which the first portion and the second portion are written to the memory unit on the same clock cycle.

5. A system comprising:

a data source;

a data target, the data target including:

a memory unit, the memory unit including:

a first memory bank; and

a second memory bank;

logic for selecting data to be written to the first memory bank, the logic being operable to select a first portion of a first block of data if the first block of data is aligned, and to select a second portion of the first block of data if the first block of data is not aligned;

logic for selecting data to be written to the second memory bank, the logic being operable to select the first portion of the first block of data if the first block of data is not aligned, and to select the second portion of the first block of data if the first block of data is aligned; and

a bus communicatively connecting the data source and the data target, the bus being operable to transfer the first block of data from the data source to the data target.

6. The system of claim 5, in which the data source comprises a microengine in a network processor.

7. The system of claim 5, in which the data target comprises a scratchpad memory in a network processor.

8. The system of claim 5, further comprising:

logic for selecting an address at which to write data to the first memory bank, the logic being operable to select a first address if the data is aligned, and to select a second address if the data is not aligned.

9. A system comprising:

a memory unit, the memory unit comprising:

a first memory bank; and

a second memory bank;

a first multiplexor, an output of the first multiplexor being communicatively connected to the first memory bank, the first multiplexor being operable to select between a first portion of a first data block and a second portion of the first data block, the selection being based on whether the first data block is aligned, and to pass the selected portion to the first memory bank;

a second multiplexor, an output of the second multiplexor being communicatively connected to the second memory bank, the second multiplexor being operable to select between the first portion of the first data block and the second portion of the first data block, the selection being based on whether the first data block is aligned, and to pass the selected portion to the second memory bank;

a third multiplexor, an output of the third multiplexor being communicatively coupled to an address input of the first memory bank, the third multiplexor being operable to select between a first address and a second address, the selection being based on whether the first data block is aligned, and to pass the selected address to the address input of the first memory bank.

10. The system of claim 9, in which the first portion of the first data block comprises the least significant bits of the first data block, and in which the second portion of the first data block comprises the most significant bits of the first data block.

11. The system of claim 9, further comprising:

bank select logic, the bank select logic being operable to determine whether a first group of data has been written to the first memory bank, and to at least temporarily disable the first memory bank from accepting additional data upon making said determination.

12. The system of claim 9, further comprising:

a FIFO memory operable to store the first data block,

the FIFO memory being communicatively coupled to a bus and operable to accept incoming blocks of data from the bus,

the FIFO memory being further communicatively coupled to the first and second multiplexors.

13. The system of claim 9, further comprising a bus, the bus having a width that is equal to the size of the first data block, the bus being operable to transfer the first data block from a master to the first and second multiplexors.

14. The system of claim 13, in which the master is designed to process blocks of data that are half the width of the first data block.

15. The system of claim 13, in which the first memory bank is half the width of the first data block, and in which the second memory bank is half the width of the first data block.

16. The system of claim 9, in which the first data block is 64-bits long.

17. The system of claim 16, further comprising a 64-bit bus, the 64-bit bus being operable to transfer the first data block from a 32-bit master to the first and second multiplexors.

18. The system of claim 17, in which the master comprises a 32-bit microengine in a network processor.

19. The system of claim 18, in which the memory unit comprises a scratchpad memory in the network processor.

20. A method for writing data to a memory unit, the method comprising:

receiving a sequence of data blocks;

obtaining a memory address at which to start writing the data blocks;

determining whether the starting memory address is even or odd;

if the starting memory address is even;

writing a first portion of a first data block in the sequence to a first memory bank at a location identified by a first address;

writing a second portion of the first data block to a second memory bank at a location identified by the first address;

if the starting memory address is odd;

writing the first portion of the first data block to the second memory bank at a location identified by a second address;

writing the second portion of the first data block to the first memory bank at a location identified by a third address.

21. The method of claim 20, further comprising:

if the starting memory address is even;

writing a first portion of a second data block in the sequence to the first memory bank at a location identified by a fourth address;

writing a second portion of the second data block to the second memory bank at a location identified by the fourth address;

if the starting memory address is odd;

writing the first portion of the second data block to the second memory bank at a location identified by a fifth address;

writing the second portion of the second data block to the first memory bank at a location identified by a sixth address.

22. The method of claim 20, in which the first address is obtained by removing a bit from the starting address.

23. The method of claim 20, further comprising:

updating a count of the amount of data written to the memory unit; and

if the count is less than a predefined value, writing additional data to the memory unit.

24. The method of claim 20, in which the blocks in the sequence comprise 64 bits, and in which the locations in the memory banks are 32 bits wide.

25. A system comprising:

a first line card, the first line card comprising:

one or more physical layer devices;

one or more framing devices; and

one or more network processors, at least one network processor comprising:

a microengine;

a memory unit, the memory unit including:

a first memory bank;

a second memory bank; and

logic for selecting data to be written to the first memory bank, the logic being operable to select a first portion of a first block of data if the first block of data is aligned, and to select a second portion of the first block of data if the first block of data is not aligned;

logic for selecting data to be written to the second memory bank, the logic being operable to select the first portion of the first block of data if the first block of data is not aligned, and to select the second portion of the first block of data if the first block of data is aligned; and

a bus connecting the microengine and the memory unit, the bus being operable to transfer the first block of data from the microengine to the memory unit.

26. The system of claim 25, further comprising:

logic for selecting an address at which to write data to the first memory bank, the logic being operable to select a first address if the data is aligned, and to select a second address if the data is not aligned.

27. The system of claim 25, further comprising:

a second line card; and

a switch fabric operable to communicatively couple the first line card and the second line card.